

Monolithic photonic BiCMOS technology for high-speed receiver applications

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ABSTRACT

Photonic-electronic integration is a key technology to master data traffic growth and therefore an enabler of future network technologies. For some time now, a novel silicon-based photonic-electronic integration technology, photonic BiCMOS, is under development at IHP. Photonic BiCMOS is a planar technology co-integrating monolithically on a single substrate high-speed RF frontend electronics – by fully featured SiGe BiCMOS – with high-speed photonic devices such as broadband germanium detectors, modulators, and SOI nano-waveguide integrated optics. High RF capability of this electronic photonic integrated circuit (ePIC) technology is enabled by SiGe heterojunction bipolar transistors (HBTs), which are integrated with 0.25 μ m CMOS.

This contribution will review the integration of a key component, the germanium detector. The integration of germanium in the BiCMOS flow results in performance issues of electronic devices and of the detector itself. We shall present measures to overcome detrimental integration effects and present examples of recent receiver demonstrators that indicate the potential for monolithic high-speed receivers at 1550nm.

Keywords: BiCMOS, silicon photonics, Ge photodiode, receiver.

1. INTRODUCTION

Silicon-based electronic-photonic integrated circuit technology enables a high degree of integration of optoelectronic subsystems for optical communications. Merge of photonics and electronics can be done either by hybrid assembly or monolithic integration. In the first case, electronic-only chips are combined with photonic-only chips after their separate fabrication [1]. Advantage is here that a mutual interference of photonic and electronic device fabrication can easily be avoided which is a more difficult task for most monolithic integration approaches. On the other hand, monolithic integration of photonic devices, such as detectors and modulators in the frontend-of-line (FEOL) of a Si-based integrated circuit technology allows for shortest possible interconnects between photonics and electronics from which high-speed performance of electronic-photonic integrated circuits (ePIC) can greatly benefit. Moreover, monolithic electronic-photonic integration leads to shrinking form-factors and reduced assembly.

Monolithic integration of Si photonics has been pursued for some time, chiefly on base of CMOS technologies [2, 3]. However, the question arises what electronic baseline technology fulfils best future communication system requirements. Looking beyond 100G systems, baud-rates exceeding 50Gbd are needed for 400G transceivers. High-speed transistors are therefore a prerequisite for high-performance ePIC technology. A key device figure of merit is the product of transit frequency and breakdown voltage ($f_T \times BV$) in which state-of-the-art SiGe heterojunction bipolar transistors (HBTs) outperform scaled NMOS transistors, the CMOS workhorses for RF. In result, SiGe HBTs are often preferred over NMOS for high-speed analogue circuits.

SiGe BiCMOS has not only an RF performance advantage of 2-3 generations over CMOS [4], wherefore SiGe bipolar or BiCMOS technologies are presently often deployed for broadband applications in high-speed discrete photonics [5], but also provides sufficient voltage swing to drive the photonics.

The photonic BiCMOS currently under development at IHP is a new monolithic ePIC technology which combines high-performance BiCMOS technology with high-speed photonic devices for electronic-photonic submodules for next generation communication networks. Here, the main features of the new technology are described, focussing on the receiver side. Demonstrator circuits fabricated in the photonic BiCMOS technology shall be reviewed too.

2. PHOTONIC BICMOS

In the RF domain, parasitic resistances, inductances and capacitances present limits to ultimate drivability, energy efficiency and speed of ePICs. The integration of the photonic devices such as waveguides, modulators,

and Ge photodiodes in the frontend-of-line (FEOL), i.e. at the same level with transistors, allows for a strong reduction of integration related parasitics because backend-of-line (BEOL) interconnect metals are used to connect photonic devices with electronic circuits. Pad capacitances and bond-related inductances are minimized or even avoided. The co-use of the BEOL metal-stack by photonic and electronic circuits is economically favourable in comparison to dual-backend approaches where electronics and photonics are processed independently and then are co-packaged. The BEOL interconnect comprises 5 metal layers and is left unchanged by the integration process. The baseline BiCMOS process for photonic integration is a 0.25 μ m-technology [6].

2.1 Technology

Figure 1 (left) illustrates the photonic BiCMOS flow which starts with an SOI-substrate with optimum dimensions for photonic application: 220nm silicon on 2 μ m buried silicon oxide (BOX). The local-SOI approach realized with the first photonic module allows one to combine SOI-based photonic components with a bulk BiCMOS core. A cross section of the full photonic process is shown in Figure 1 on the right.

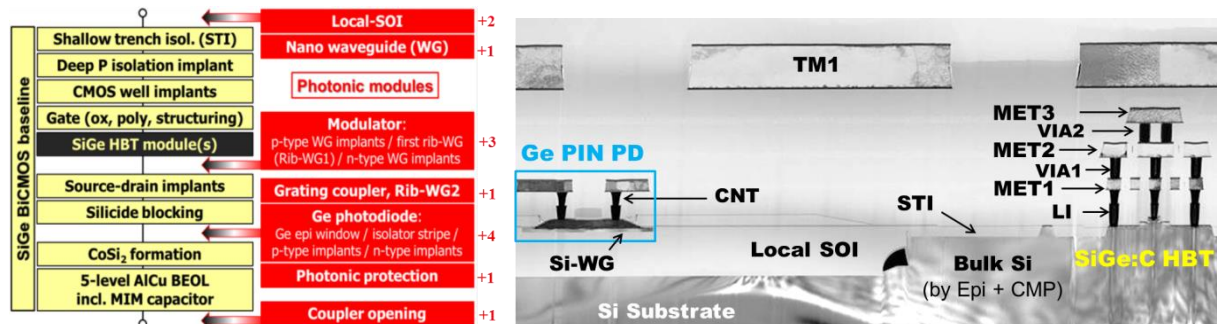


Figure 1: Photonic BiCMOS process flow (left): Photonic modules are integrated in a SiGe BiCMOS baseline process. The numbers beside the photonic modules indicate the additional mask steps for the photonic functionality. Photonic BiCMOS cross-section (right): A first-generation Ge lateral p-i-n PD and a SiGe-HBT are shown (cut perpendicular to the direction of light propagation).

The conflicting substrate requirements of BiCMOS and photonics are resolved by a mixed substrate technology, the local-SOI approach [7], which is realized with the first photonic module and is illustrated in Figure 1 (right).

2.2 Photo Detector Integration

A core device of the new photonic BiCMOS process is an integrated Ge p-i-n photodiode (Ge-PD). Based on a first PD generation with about 30GHz bandwidth and 0.8A/W responsivity, a new, much improved Ge-PD was integrated in the process [8]. Compared to the first one, the latter offers more than two times higher bandwidth and about 30% higher responsivity. The process flow of the detector module is illustrated in Figure 2. The new diode structure results of a layout variation only, i.e. its fabrication does not need any process changes compared to the old device.

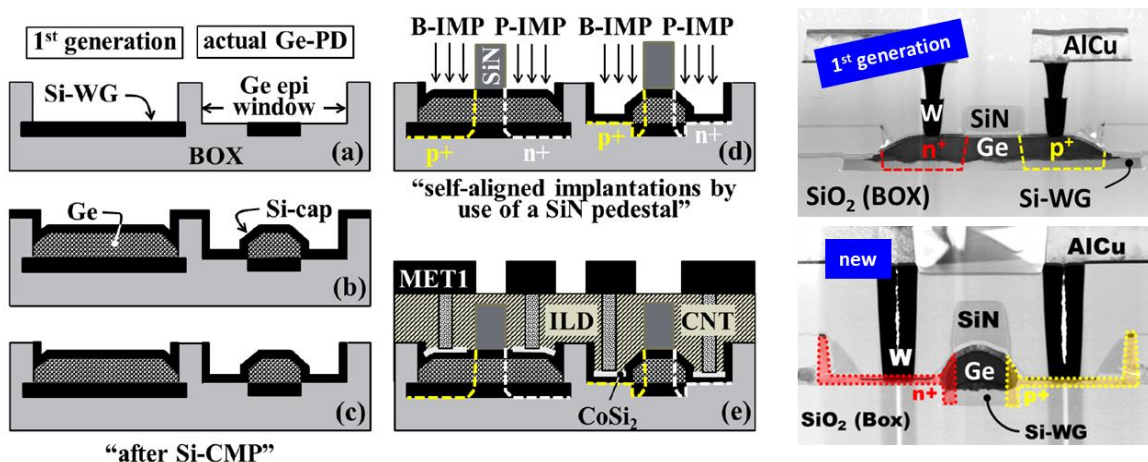


Figure 2: Fabrication flow for first and latest Ge-PD generation (left) and TEM cross sections for both detector generations (right). Cut perpendicular to the direction of light incidence.

Small signal frequency response measurements were performed at zero-bias and under reverse bias of 2V. The increase in the -3 dB bandwidth under all bias conditions is quite obvious when comparing the new to the previous detector generation (Figure 3, left). The bandwidth improvement results from a reduction of the lateral dimensions of the doped Ge regions and the incorporation of non-doping implants that were used for diffusion length manipulation [9]. Both measures lower the impact of “slow” photo carrier diffusion. The first measure also reduces free carrier absorption. The separation of the absorption (Ge) from contact regions (Si) in the new diode structure also prevents metal absorption. Both measures are beneficial for the responsivity. Responsivity values for C- and L-bands are shown in Figure 3, on the right side.

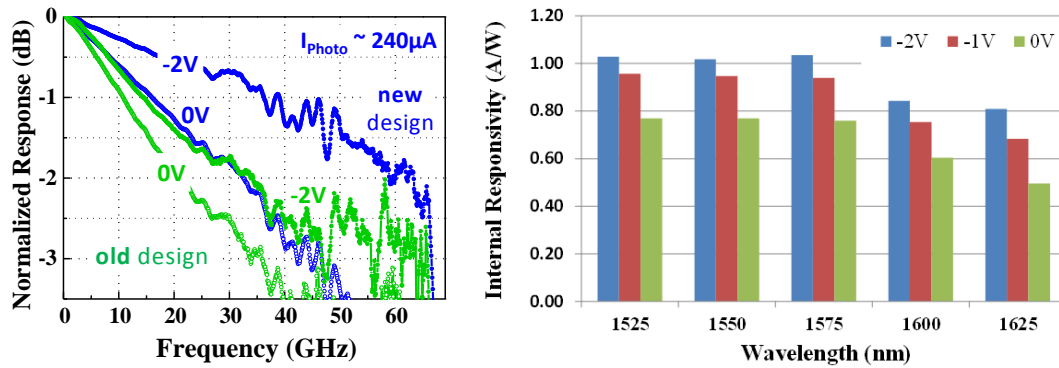


Figure 3: Normalized frequency response of the previous and the new photo detector generations, obtained from small-signal measurements (67GHz LWCA, 1.55 μ m)(left) and internal responsivity of the new detector across C- and L-band (right).

The diodes are fabricated from a Ge layer, selectively grown on a Si waveguide. The epitaxy is carried out after the BiCMOS source-drain anneal ($T_{Peak} > 1000^{\circ}C$), but before the cobalt silicide module. In this way melting of the Ge layer and mixing it with underlying Si material is prevented. Moreover, any metal contamination of tools used for Ge epitaxy and pre-epitaxy wet cleaning is excluded. B and P implantation steps applied to form the lateral p-i-n structure are also carried out before silicide formation. Due to the thermal budget required for the $CoSi_2$ formation, the fabrication of a PD with steep doping profiles necessary to get a bandwidth of 40GHz or more becomes very challenging. Nonetheless, by lowering the anneal temperature of the $CoSi_2$ module in photonic BiCMOS in comparison to that of the baseline, photodiodes with high bandwidth were realized. It was shown that this change can be done in a way that prevents negative effects on the BiCMOS devices, in particular on the SiGe HBT RF performance [10].

As mentioned above, Ge epitaxy is carried out after the BiCMOS source-drain annealing (SD-RTA). To get directly on a Si waveguide a Ge layer with low defect density as a prerequisite for low diode dark currents, layer deposition is carried out after a pre-bake step and under use of a cyclic annealing applied during the layer growth [11]. This additional thermal budget leads to several effects: First, dopant de-activation increases the SiGe HBT base resistance and thus strongly lowers maximum oscillation frequency (f_{max}). By replacing the baseline SD-RTA by a spike-anneal (with higher temperature but shorter anneal time) dopant activation is improved and dopant diffusion is lowered. The measurement results shown in Figure 4 prove that the problem of f_{max} degradation due to PD integration could be fixed, which is also confirmed by the ring oscillator data shown right next to it. The gate delay mean value of 4.0ps matches very well the corresponding baseline SG25H1 BiCMOS value.

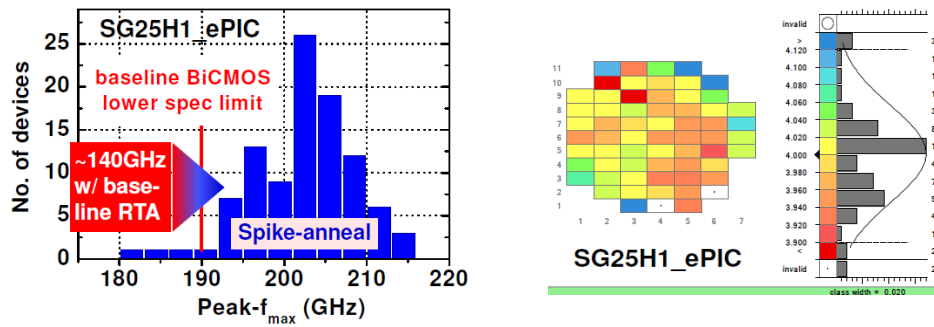


Figure 4: Histogram of f_{\max} values (extrapolated from de-embedded unilateral gain vs. frequency) obtained for SiGe HBTs (left) and distribution with histogram of SiGe HBT ring oscillator delay times measured on wafers from a photonic BiCMOS run (right).

Besides degraded f_{\max} values, also polysilicon resistors deviate from the baseline specification and the threshold voltage of the PMOS transistors were strongly reduced. Further, increased dopant diffusion has a negative effect in particular on the NMOS transistor short-channel V_{th} behaviour. The following measures to counter these effects were applied: an increased NWELL doping level improved the PMOS behaviour and a reduction of the NMOS source-drain implantation dose improved the NMOS behaviour.

In result, the photonic BiCMOS device behaviour is now quite close to that of the baseline which enables the re-use of the baseline-PDK for the BiCMOS devices of the ePIC process.

2.3 Monolithically Integrated Receivers

Monolithically integrated receivers for data rates beyond 40 Gbps were designed, fabricated and characterized. Amongst these was, to our knowledge, the first monolithically integrated Si-based ePIC receiver for 56 Gbps [12]. A chip photo of this IC and eye diagrams can be seen from Figure 5.

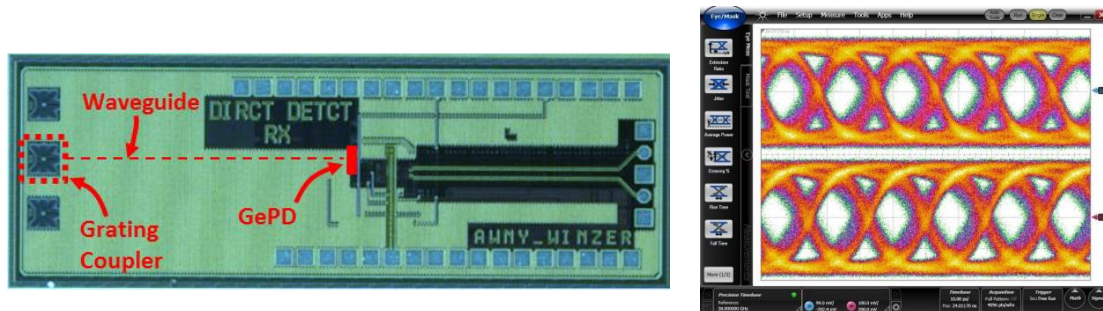


Figure 5: Chip photograph of a monolithically integrated linear direct detection receiver realized in IHP's photonic BiCMOS process (left) and eye diagrams for received $2^{31}-1$ PRBS data sequence at 56Gbps OOK NRZ (x,y scale: 10ps/div, 100mV/div) (right) [12].

3. CONCLUSIONS

This contribution reviewed the integration of the Ge detector, a key component of IHP's novel photonic BiCMOS process. Performance issues of electronic devices and of the germanium detector itself were discussed and countermeasures were presented. Recent demonstrators indicate the potential for monolithic high-speed receivers at 1550nm.

ACKNOWLEDGEMENTS

This project has received funding by one of the calls under the Photonics Public Private Partnership from the European Union's Horizon 2020 research and innovation programme under grant agreement No 688003. The authors also gratefully acknowledge partial support by German Ministry of Research and Education (BMBF), project SPEED.

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