# Monolithically Integrated MZM with Segmented Driver in Photonic BiCMOS showing High ER

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***Abstract*—In this work, a dual-drive Si depletion-type MZM monolithically integrated with a segmented driver using 0.25 μm SiGe:C photonic BiCMOS technology is demonstrated. The phase shifter on each MZM arm has a total length of 6.048 mm and is divided into 16 sections which are driven by the driver segments. Electro-optic time-domain measurements show extinction ratio higher than 11 dB at 28 and 32 Gb/s at OOK with a differential input voltage swing equal to 800 $mV_{pp}$ (3.5 $V_{pp}$ on the phase shifters). This is one of the highest extinction ratio values shown by a monolithically integrated Si MZM at those data rates. The driver dissipates a total DC power equal to 64 pJ/bit at 28 Gb/s.**

***Index Terms*—optical transmitters, silicon, integrated optoelectronics.**

## I. Introduction

With the advance of optical networks, the corresponding bandwidth demands increase rapidly. To meet those requirements complex transmitter and receiver architectures are developed. Silicon (Si) photonics has drawn significant attention mainly because of the need for a technology platform that enables the integration of the photonic with the electronic components which is a key feature toward the realization of high-speed systems [1], [2]. From the transmitter side, Si depletion type Mach-Zehnder modulators (MZMs) are considered promising candidates for this technology mainly because of their large intrinsic bandwidth and simplicity in fabrication [3], [4]. Most Si-based MZMs are using traveling-wave electrodes (TWEs) to achieve high-speed operation [5], [6]. Their major drawback is however the large voltage required in order to be driven efficiently. However, using electronic-photonic integration technology, the driver can be placed in close proximity to the modulator, thus eliminating the need for an additional radio frequency (RF) broadband amplifier.

From the different integration platforms, the monolithic integration of optical and electrical components is considered particularly attractive. This is because it allows the implementation of the photonic devices in the immediate vicinity of the transistors, enabling the shortest possible electrical interconnects between electronics and photonics which benefits the high-speed performance of the integrated circuits. IHP′s photonic-electronic platform is using SiGe bipolar complementary metal oxide semiconductor (BiCMOS) technology combined with the photonic circuits. In this way, the MZM can be integrated in the frontend of a high performance BiCMOS technology with fast heterojunction bipolar transistors (HBTs) with $f_T$ of about 190 GHz and breakdown voltage up to 1.9 V [7]. On the driver side, such a BiCMOS technology can provide large driving voltage at high speed, offering the possibility to fully drive the MZMs which is often not the case in complementary metal oxide semiconductor (CMOS) technologies where low breakdown voltage is the trade-off to high $f_T$. The drawback of BiCMOS compared to CMOS is, however, the larger power consumption [2].

The driver design is based on the segmented driver approach in which the driver is distributed along the phase shifter known as segmented MZM (SE-MZM) concept. The expected advantage of the Se-MZM is the high extinction ratio (ER) since the RF voltage is kept constant along the phase shifter due to the isolation of the transmission line from the phase shifter thus minimizing the microwave loss that decrease the effective voltage on the phase shifters when using TWE design [8]. Using this topology the modulator bandwidth is expected to be independent of the phase shifter length and it will only depend on its RC constant which is typically small enough to provide high-speed operation. Moreover good velocity matching can be achieved which is a critical issue when using long phase shifters.

In our previous work we had demonstrated our monolithic integration concept by presenting a 10 Gb/s MZM with driver [9]. However, that device had limited speed and ER due to transmission line-based driver design and small phase shifter length, thus resulting in large $V_\pi$. In the current work we demonstrate the SE-MZM concept on long Si modulators (6 mm) that offers the possibility to minimize the driving voltage without sacrificing available bandwidth. 28 and 32 Gb/s on-off keying (OOK) operation is presented showing more than 11 dB ER with differential input voltage swing equal to 800 $mV_{pp}$. Such a low value of input voltage makes our device compatible with commercial digital-to-analog converters (DACs). The ER of the SE-MZM presented here is as high as the one reported previously using also monolithic integration [1] and at the

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same time it is operated at higher data rates.

## II. Device Description

The circuit is fabricated using IHP's 0.25 μm SiGe:C BiCMOS process. Initially an 8 inch silicon-on-insulator (SOI) wafer with a top Si layer of 220 nm and a buried oxide (BOX) layer of 2 μm is used. Then a module called 'local SOI' is implemented in the process flow to produce SOI and bulk regions located close to each other [7]. The SOI areas are used for the fabrication of the photonic components while the electronic devices are formed on bulk Si regions. In Fig. 1 a microphotograph of the monolithically integrated SE-MZM is shown where all the main chip components are noted. The chip area is approximately 12.7 mm$^2$ (9.8 mm x 1.3 mm).

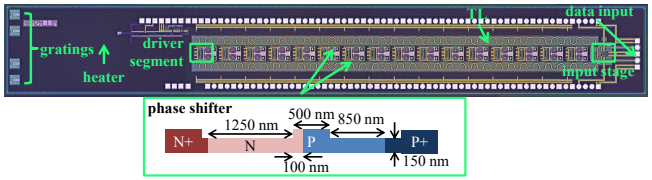


Fig. 1: Microphotograph of the monolithically integrated Si SE-MZM.

### A. MZM

The device is based on a dual-drive symmetric MZM structure. Each arm has a length of 6.08 mm and is divided into 16 segments, each of which has an active length of 378 μm resulting in a total phase shifter length of 6.048 mm. The separation between the segments is equal to 2 μm. Each phase shifter segment (378 μm) can be considered as a lumped element for data rates up to 40 Gb/s and is driven by a separate driver. The phase shifter is based on a PN junction formed inside the waveguide using self-aligned process. With this technique larger confinement between the optical mode and the depletion region can be achieved without increasing the complexity of the process. The target boron doping concentration is chosen to be equal to $3{\cdot}10^{17}$ cm$^{-3}$ while arsenic doping concentration is targeted at $1{\cdot}10^{18}$ cm$^{-3}$. From Fig. 2 it is seen that when the reverse bias voltage ($V_{bias}$) is equal to 1 V, the phase shifter shows $V_\pi \cdot L$ of the order of 2.7 V·cm. This means that for phase shifter length equal to 6.048 mm the $V_\pi$ is approximately 4.5 V.

The highly-doped regions are placed at a theoretically optimized distance from the waveguide core to not cause additional absorption loss (Fig. 1). At the p-side the distance to the highly-doped region is designed to be smaller than the n-side because of being lower-doped thus resulting in larger resistivity at the p-side. A series resistance of approximately 50 Ω is estimated per segment for both the p- and n-doped regions (resistivity of 1.9 Ω· cm). The total fiber-to-fiber optical loss is of the order of 19 dB. The insertion loss due to the phase shifter itself is estimated to be approximately 6 dB. For coupling the light in and out from the chip two standard grating couplers are used which are responsible for approximately 8 dB loss (4 dB each). The remaining loss can be attributed to the multimode interference (MMIs) devices, the waveguide parts that connect the optical components as well as the 1.5 mm long heaters designed to provide DC tuning.

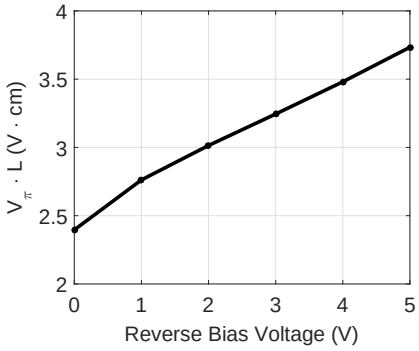


Fig. 2: Phase shifter inverse efficiency $V_\pi \cdot L$ extracted from measurements.

### B. Segmented Driver

A block diagram of the integrated transmitter is shown in Fig. 3. The driver amplifier part integrates two stages. The input stage which is matched to 50 Ω, drives a differential signal to two single-ended transmission lines and has a gain of 1 dB. The second stage is distributed laterally to the modulator segments. Each driver segment senses the differential voltage from the lines, amplifies it by 12 dB and applies it to each modulator section. The modulator section is the driver load that is represented by its equivalent electrical model, the phase shifter depletion capacitance and the series resistance. This RC load determines mainly the MZM bandwidth. Each driver segment dissipates power equal to almost 110 mW. The driver is strategically positioned between the MZM arms for symmetry reasons.

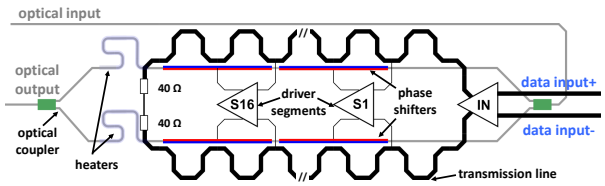


Fig. 3: Block diagram of the integrated Se-MZM transmitter.

The simulated optical group index and the electrical microwave index are equal to 3.6 and 2.1 respectively. Because of the difference in the velocities, in order to optimize the MZM' s electro-optic (EO) response the transmission lines are properly folded to create an artificial delay to the electrical signal. Using this technique the timing difference of both waves between segments is theoretically matched to a value of 4.6 ps. Furthermore, to minimize the electrical loss due to the transmission line, its characteristic impedance is designed to be 40 Ω. This impedance results into wider lines with less microwave loss than the conventional 50 Ω. The lines are terminated with resistors with the same resistance value. Since the lines are now isolated from the load their microwave

loss is significantly lower than the conventional TWE approach. Furthermore, in order to compensate the remaining transmission line loss towards the last segments, more gain is added progressively. More details about the electrical circuit are described in our previous work [10].

## III. Co-Simulation Technique

The integrated SE-MZM system is simulated as follows. The optical depletion-type phase shifter is modeled by using device simulation tools as described previously [11]. With this technique the refractive index as well as the phase shifter absorption loss change with applied voltage are calculated. The values of the depletion capacitance and the series resistance are also estimated using Sentaurus TCAD. In Fig. 4 the measured and simulated depletion capacitance change with applied voltage is shown. The measurement curve represents multiple chips in order to show the deviation from the simulated curve. The optical delay is also calculated so as to analyze the effects of velocity mismatch. After having calculated all these parameters the phase shifter can be treated as an optical component described by the above properties.

In the next step the optical components such as phase shifters, MMIs and DC tuning sections are implemented into a standard electronic design platform such as Cadence Virtuoso by creating instances using VerilogA. VerilogA models for optical components have already been shown [12]. The segmented driver is also simulated by using Cadence Virtuoso and consequently the optical and electrical components are easily combined together so as to predict the modulator EO response.

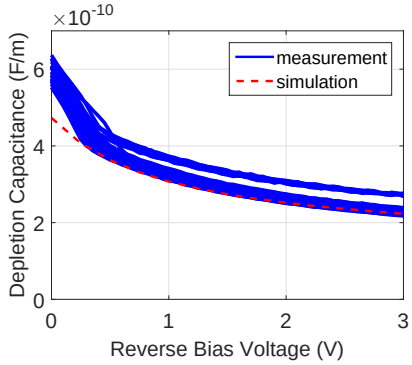


Fig. 4: Phase shifter depletion capacitance change with reverse bias voltage.

## IV. Measurement Results

The EO frequency response of the SE-MZM is characterized using a Keysight 67 GHz lightwave component analyzer (LCA). The measurements are performed on wafer with a 67 GHz GSGSG RF probe. The MZM EO $S_{21}$ is depicted in Fig. 5. A 3 dB bandwidth of approximately 18 GHz is measured when the reverse bias voltage ($V_{bias}$) is equal to 1 V. By changing the bias voltage of the modulator the bandwidth increases due to the depletion capacitance reduction. The reason for the peaking observed at high frequencies can be related to the bandwidth enhancing technique used in the driver.

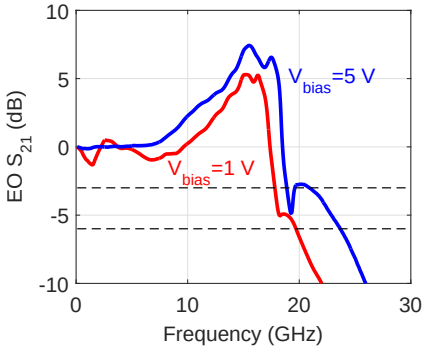


Fig. 5: Normalized measured EO $S_{21}$ with frequency when $V_{bias}$ is equal to 1 and 5 V.

For the optical eye-diagram measurement a bit pattern generator provides a $2^{31}$-1 pseudo random binary sequence (PRBS). The differential output is connected to the modulator RF input which is driven push-pull for OOK demonstration. This differential voltage has an amplitude equal to 800 $mV_{pp}$ and with a total gain of 13 dB it results in differential voltage equal to 3.5 $V_{pp}$ applied to the phase shifters. At the optical input a continuous wave (CW) laser signal was injected. At the optical output an erbium-doped fiber amplifier (EDFA) is used to amplify the signal for subsequent evaluation. For the eye measurements of the generated data sequence a photodetector is connected to the input of a sampling head of an oscilloscope. Photodetector and sampling head have a bandwidth of 50 and 70 GHz respectively.

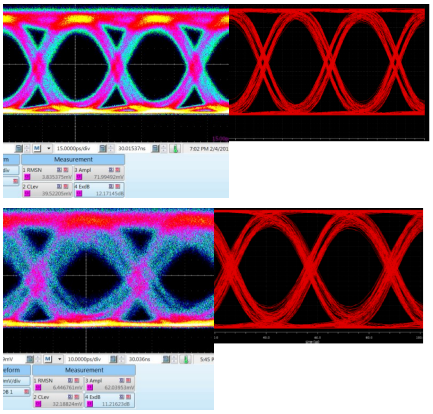

Fig. 6: Measured (left) and simulated (right) EO eye-diagrams at 28 (top) and 32 Gb/s (bottom) using PRBS31 when $V_{bias}$ is equal to 1 V.

In Fig. 6 the measured as well as the co-simulated optical eye diagrams at 28 and 32 Gb/s are shown when $V_{bias}$ is equal to 1 V. The jitter noticed at 32 Gb/s is due to the limited bandwidth at this data rate. Good agreement between measured eye-diagrams and simulation proves the accuracy of the co-simulation technique. ER 12.0 and 11.0 dB is measured at 28 and 32 Gb/s respectively. The high value of ER is among the

highest reported among integrated Si modulators at this data rate [1], [2], [8] and can be attributed to the fact that the long phase shifter (6.048 mm) enabled to almost fully drive the MZM since the 3.5 $V_{pp}$ correspond to almost 80% of the $V_\pi$. Higher values of reverse bias voltage were also tested because they are expected to increase the MZM cut-off frequency (Fig. 5) [13]. However due to the trade-off between bandwidth and phase shifter efficiency with reverse bias voltage (Fig. 2) a significant reduction in the ER is observed for large values of $V_{bias}$ (Fig. 7). The total power consumption of the device is equal to 1.8 W or 64 pJ/bit at 28 Gb/s. This large value of power dissipation is the trade-off to the large number of segments that are necessary to demonstrate high ER. Moreover, the driver incorporates a linear topology so that when attached to a high-speed DAC, it can enable the demonstration of higher order modulation formats [14].

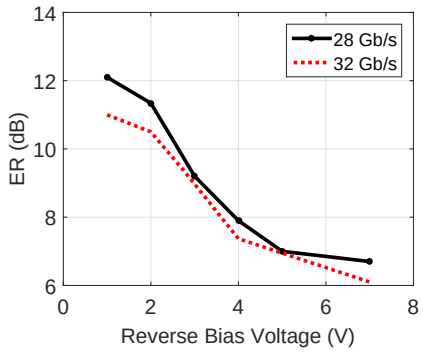


Fig. 7: ER change with reverse bias voltage at 28 and 32 Gb/s.

## V. Conclusions

A monolithically integrated Si depletion-type MZM with a linear segmented driver in IHP's photonic BiCMOS process is demonstrated. High ER is measured at 28 and 32 Gb/s indicating that our device performance is comparable to state-of-the-art monolothically integrated MZMs [1]. The high ER together with the linear driver topology are crucial for the future demonstration of higher order modulation formats [15]. The trade-off to the driver's linear functionality as well as the large number of segments required to demonstrate high ER is clearly the large power consumption (1.8 W). Regarding further device optimization, a decrease in the loss figure is required in order to make our device competitive towards other technologies. Our simulations predict that by optimizing the process as well as the phase shifter design a total MZM loss of the order of 10 dB can be expected. In terms of speed, our device could be further optimized by using a photonic BiCMOS technology with faster bipolar transistors [16] and by reducing the phase shifter series resistance with the implementation of additional doping masks in our process [5]. Our simulation indicates that such a SE-MZM design could enable transmission data rates higher than 40 Gb/s at OOK.

## Acknowledgments

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